

## SPECIFICATION

### TITLE OF THE INVENTION

A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND  
A METHOD OF MANUFACTURING THE SAME

This invention relates to a semiconductor integrated circuit device and also to a technique of manufacturing the same. More particularly, the invention relates to a technique which is effective for application to wirings formed by a so-called damascene method wherein after formation of grooves for wirings in an insulating film a conductive film is buried inside the grooves.

### BACKGROUND OF THE INVENTION

In recent years, as scaling-down and multi-layered formation of wirings of a semiconductor integrated circuit device are in progress, a so-called damacene technique has been studied, as described, for example, by T. Saito et. al., in Proceedings of International Interconnect Technology Conference in 1998, pp. 160 - 162 and the like, in which after formation of a groove for wirings in an insulating film, a conductive film is buried inside the groove.

In Japanese laid-open patent Application No. Hei 8(1996)-222568, there is described a technique wherein a groove for wiring is formed in an insulating film and a barrier layer made of a TiN (titanium nitride) thin film is formed according

to a CVD (chemical vapor deposition) method, after which a copper thin film is formed on the barrier layer and the copper thin film is etched back, followed by further formation of a protective film made of a TiN thin film and subsequent etching to leave the protective film on the resultant copper thin film wiring.

In the technical report of Mitsubishi Electric Corporation in 1997, pp333-336, there is described a technique wherein a barrier layer such as TiWN or the like is provided on the upper surface of a copper damascene wiring.

#### SUMMARY OF THE INVENTION

We have recognized the following problem involved in a technique not known in the art when wirings are formed according to the so-called damascene technique wherein after formation of a groove for wiring in such an insulating film as mentioned above, a conductive film is buried inside the groove to form a wiring.

For instance, ~~copper~~ is usually used as the conductive film. Copper (Cu) has such a property that when compared with other metals such as aluminium (Al), tungsten (W) and the like, copper is more liable to be diffused into a silicon oxide film used as the insulating film. When a silicon oxide film is formed directly on the conductive film, the copper at the contact portion is oxidized, thereby permitting the wiring resistance to rise.

Accordingly, a study on a barrier layer covering the wiring therewith becomes important. Of the barrier films covering the

wiring, a titanium nitride (TiN) film has been studied with respect to the barrier film formed inside the groove for wiring. Likewise, silicon nitride (SiN) has been studied for use as a film (cap film) covering the upper portion of the wiring.

However, in order to prevent the diffusion and oxidation of copper by means of the silicon nitride film covering the wiring on the upper portion thereof, it is necessary that the silicon nitride film be formed in a certain thickness. Since the silicon nitride film has a high dielectric constant, the RC time constant of the wiring becomes great, thereby impeding the high-speed operation of a device.

Electromigration may occur owing to the diffusion of copper inside the copper wiring or at the copper surface. As a result of our study on the ease in the diffusion of copper, it was supposed that when a copper-barrier film interface was compared with a copper-silicon nitride film interface, the activation energy of diffusion at the copper-barrier film interface was greater (i.e. copper was more unlikely to be diffused at the copper-barrier film interface). Accordingly, the electromigration life is determined by the activation energy value of diffusion of copper at the copper-silicon oxide film interface.

Where an upper wiring is further formed on the copper wiring through an insulating film wherein the copper wiring and the upper wiring are connected with each other through a plug

formed in the insulating film, the silicon nitride film over the copper wiring has been removed so as to permit the contact, under which the bottom surface of the plug is in direct contact with the copper of the lower wiring. This is liable to cause the concentration of an electric current through the current path from the plug bottom to the lower copper wiring, thereby causing electromigration to occur. Moreover, when voids are formed beneath the plug by the influence of the electromigration, the area of contact between the plug and the lower copper wiring becomes small, thereby leading to the accelerated lowering of the wiring life.

When the plug is formed, a contact hole is also made. In this case or when the contact hole is etched at the bottom thereof so as to improve the contact characteristic, the copper wiring per se at the bottom of the contact hole is also sputter-etched. This allows copper to be deposited on side walls of the contact hole. As set out hereinabove, such copper is liable to be diffused in the insulating film, thus bringing about the lowering of breakdown voltage and an increased leakage current.

For burying the conductive film in the groove for wiring, a copper film is, for example, formed on the insulating film including the inner portion of the groove for wiring, followed by removal an additional copper film outside the group by chemical mechanical polishing (CMP). At that time, it may be inevitable that recesses or other defects occur. Thereafter, when a silicon

nitride film is formed on the copper wiring, voids are formed at the defective portions, with the possibility that electromigration is undesirably caused to start from the void.

Further, where a mask for the contact hole is shifted relative to the lower copper wiring, a fine recess may occur at a side portion of the lower wiring. It is difficult to bury a plug in such a fine recess, thus leading to the formation of a void like the above case, with the possibility of creating a starting point for electromigration. In this case, because an area of contact between the plug and the lower wiring is reduced owing to the shifting of the mask, under which when the void is moved toward the interface of the contact, the connection between the plug and the lower wiring is not ensured, resulting in connection failure.

It is accordingly an object of the invention to provide a semiconductor integrated circuit device and a manufacturing method thereof wherein a cap conductive film is formed on a wiring, thereby realizing the high speed operation of the device.

It is another object of the invention to provide a semiconductor integrated circuit device and a manufacturing method thereof wherein an elongated wiring life is ensured while suppressing electromigration and stress migration from occurring.

It is a further object of the invention to provide a semiconductor integrated circuit device and a manufacturing

method thereof wherein the device is improved in dielectric breakdown and has a reduced leakage current by preventing direct sputtering of an underlying copper wiring when a contact hole is etched at the bottom thereof.

It is a still further object of the invention to provide a semiconductor integrated circuit device and a manufacturing method thereof wherein contact failure is reduced in contact failure if a contact hole is shifted relative to a wiring.

The above objects and novel features of the invention will become apparent from the description of the specification and the accompanying drawings.

Typical embodiments of the invention are summarized below.

The method for manufacturing a semiconductor integrated circuit device according to the invention comprises successively forming a barrier layer and a conductive layer within a groove for wiring, removing the barrier layer and the conductive film from outside of the groove for wiring to form a wiring, and forming a cap conductive film on the wiring by selective or preferential growth.

When the cap conductive film is formed on the wiring by selective or preferential growth in this way, the formation of the cap conductive film becomes easy, thus enabling one to realize a high-speed semiconductor integrated circuit device. Moreover, occurrence of electromigration or stress migration can be



film or the like. For the low dielectric insulating film, there is used, for example, a TEOS film or an SiOF film.

Prior to the formation of the cap conductive film, the substrate surface may be cleaned with a solution containing hydrogen fluoride or the like for removing foreign matters or a contaminated metal. Alternatively, prior to the formation of the cap conductive film, the substrate surface may be treated with hydrogen. After the formation of the cap conductive film, the substrate surface may be cleaned with a solution containing hydrogen fluoride (HF) or hydrogen peroxide ( $H_2O_2$ ).

As a result of these treatments, there can be formed a highly reliable cap conductive film.

The semiconductor integrated circuit device of the invention comprises a barrier layer formed at side walls and bottom of a groove for wiring, a conductive film formed on the barrier layer, and a cap conductive film formed on the conductive film.

The formation of the cap conductive film on the conductive film (wiring) in this way ensures the provision of a high-speed semiconductor integrated circuit device. Moreover, the occurrence of electromigration or stress migration can be suppressed, resulting in the elongated life of the wiring. In addition, when a contact hole formed on the wiring is etched at the bottom thereof, the direct sputtering of the underlying wiring can be prevented, thus realizing the improvement of



dielectric breakdown and the reduction of leakage current. If the contact hole is shifted relative to the wiring, the contact can be maintained, and thus, contact failure can be reduced in number.

It will be noted that the wiring is made, for example, of copper, silver, aluminium or an alloy containing these metals as a main component. The cap conductive film is, for example, a W film. The cap conductive film may be a film of WN, TiN, Ta, TaN or Ni. Alternatively, the cap conductive film may be a film which is formed by selective growth or preferential growth, or may be a film which is formed at a pressure of 1 Torr ( $1 \times 1.33322 \times 10^2$  Pa) or below. The thickness of the cap conductive film should be uniform within the same plane of the wiring and can be made uniform irrespective of the wiring width. The variation of the thickness of the cap conductive film may be within a range of 50% or below. Moreover, the thickness of the cap conductive film can be made thinner than the barrier layer at the bottom of the groove for wiring. More particularly, the thickness of the cap conductive film ranges, for example, from 2 to 20 nm.

The insulating film on the cap conductive film may be made of a laminated film including a TEOS film or carbon-containing silicon insulating film and a film whose dielectric constant is lower than the first-mentioned one. Alternatively, the insulating film on the cap conductive film may be made of a diffusion-preventing insulating film for preventing diffusion

of a conductor material for the conductive film, and a low dielectric insulating film. For the diffusion-preventing insulating film, there is used, for example, a silicon nitride film, a PSG film or a silicon carbide film. For the low dielectric insulating film, there is used, for example, a TEOS film or an SiOF film.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1a and 1b are, respectively, a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Figs. 2a and 2b are, respectively, a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Figs. 3a and 3b are, respectively, a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Fig. 4a and 4b are, respectively, a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Figs. 5a and 5b are, respectively, a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Figs. 6a and 6b are, respectively, a sectional view showing the step of manufacturing a semiconductor integrated circuit

device according Embodiment 1 of the invention;

Figs. 7a and 7b are, respectively, a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Figs. 8a and 8b are, respectively, a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Fig. 9 is a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Fig. 10 is a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Fig. 11 is a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Fig. 12 is a sectional view showing the step of manufacturing a semiconductor integrated circuit device according Embodiment 1 of the invention;

Figs. 13a and 13b are, respectively a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 2 of the invention;

Figs. 14a and 14b are, respectively a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 2 of the invention;

Figs. 15a and 15b are, respectively a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 2 of the invention;

Figs. 16a and 16b are, respectively a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 2 of the invention;

Figs. 17a and 17b are, respectively a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 2 of the invention;

Figs. 18a and 18b are, respectively a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 2 of the invention;

Fig. 19 is a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 2 of the invention;

Fig. 20 is a sectional view showing the step of manufacturing a semiconductor-integrated circuit device according to Embodiment 2 of the invention;

Fig. 21 is a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 2 of the invention;

Figs. 22a and 22b are, respectively, a sectional view illustrating the effect of the invention;

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Figs. 24a and 24b are, respectively, a sectional view illustrating the effect of the invention;

Figs. 25a and 25b are, respectively a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 3 of the invention;

Figs. 26a and 26b are, respectively a sectional view showing the step of manufacturing a semiconductor integrated circuit device according to Embodiment 4 of the invention;

Figs. 27a, 27b and 27c are, respectively, a sectional view illustrating the effect concerning Embodiments 5 and 7 of the invention;

Figs. 27a, 27b and 27c are, respectively, a sectional view illustrating the effect concerning Embodiments 5 and 7 of the invention;

Figs. 28a, 28b and 28c are, respectively, a sectional view illustrating the effect concerning Embodiments 5 and 6 of the invention;

Fig. 29 is a view illustrating the effect of the invention;  
and

Figs. 30a, 30b and 30c are, respectively, a view showing the step of manufacturing a semiconductor integrated circuit device according to another embodiment of the invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the invention are described in detail with reference to the accompanying drawings. It should be noted that like reference numerals indicate like members throughout the drawings illustrating the embodiments and are not repeatedly illustrated.

(Embodiment 1)

Figs. 1a and 1b to 1l are, respectively, a sectional view showing the successive steps of a method of manufacturing a semiconductor integrated circuit device according to Embodiment 1 of the invention.

As shown in Fig. 1a, a semiconductor substrate 1 made, for example of p-type single crystal silicon is provided, and an element isolation region 2 is formed on the main surface of the semiconductor substrate 1. For the formation of the element isolation region 2, the semiconductor substrate 1 is etched at the element isolation region thereof to form an approximately 350 nm thick groove, followed by thermal oxidation of the semiconductor substrate 1 at about 850 to 1000°C to form an approximately 10 nm thick silicon oxide film (not shown) on the inner walls of the groove. Next, a silicon oxide film having a thickness of approximately 45 to 500 nm is deposited on the semiconductor substrate 1 including the inside of the groove according to a CVD method. Thereafter, the silicon oxide film outside the groove is removed by CMP to flatten the surface.

Thereafter, a p-type impurity (e.g. boron (B)) and an n-type impurity (e.g. phosphorus (P)) are, respectively, ion-implanted into the semiconductor substrate 1, and the semiconductor substrate is thermally treated at about 950°C to diffuse the impurities, thereby forming a p-type well 3 and an n-type well 4.

Subsequently, as shown in Fig. 1b, the semiconductor substrate 1 is cleaned on the surface thereof by wet etching using, for example, hydrofluoric acid, and is subsequently thermally oxidized at about 800 to 850°C to form a clean gate oxide film 5 having a thickness of approximately 7 nm on the surface thereof.

Next, a polysilicon film 6 is, for example, formed and etched to form a gate electrode 7 as shown in Fig. 2a. At the time, an n-type impurity (e.g. phosphorus) is injected into the polysilicon 6 on the p-type well 3, and a p-type impurity (e.g. boron) is injected into the polysilicon 6 on the n-type well 4, thus making it possible to provide a so-called dual gate structure wherein the gate electrode of the n-channel MISFET is of the n type and the gate electrode of the p-channel MISFET is of the p type. The adoption of the dual gate structure enables one to lower the threshold value ( $V_{th}$ ) of the MISFET and drive the MISFET at low voltage.

Thereafter, as shown in Fig. 2b, an n-type impurity (phosphorus (P) or arsenic (As)) is ion-implanted into the semiconductor substrate 1 at opposite sides of the gate electrode

7 on the p-type well 3, thereby forming n-type semiconductor regions 8 (source, drain). Likewise, a p-type impurity (e.g. boron) is ion-implanted into the semiconductor substrate 1 at opposite sides of the gate electrode 7 on the n-type well 4, thereby forming p-type semiconductor regions (source, drain).

Subsequently, a side wall 10 is formed on side walls of the gate electrode 7. The side wall 10 is formed by depositing an approximately 50 to 100 nm thick silicon nitride film, serving as an insulating film, on the semiconductor substrate 1 by a CVD method and anisotropically etching the silicon nitride film. The insulating film may be constituted of a silicon oxide film.

While using the gate electrode 7 and the side wall 10 as a mask (i.e. in a self-aligned way), an n-type impurity (phosphorus or arsenic) is ion-implanted into the p-type well 3 to form n<sup>+</sup>-type semiconductor regions 11 (source, drain), and a p-type impurity (boron) is ion implanted into the n-type well 4 to form p<sup>+</sup>-type semiconductor regions 12 (source, drain).

According to these steps set out hereinabove, there can be obtained an n-channel MISFETQn and a p-channel MISFETQp, each provided with the source and drain having an LDD (lightly doped drain) structure.

Next, as shown in Fig. 3a, a resistor element is formed on the wide element isolation region 2. This resistor element includes a conductor film R, an insulating film 13 covering the conductor film R and a lead electrode 14 on the insulating film



13 and is formed in the following manner. For instance, a conductor film such as of polysilicon or the like, into which an impurity is introduced in a reduced amount, is deposited over the entire surface of the semiconductor substrate 1, followed by patterning to form the conductor film R. This conductor film R may be made, aside from the semiconductor film such as polysilicon film, of a metal film such as tungsten or the like.

Next, an insulating film 13 such as a silicon oxide, a silicon nitride film or the like, is deposited on the conductor film R by a CVD (chemical vapor deposition) method or a sputtering method.

Further, part of the insulating film 13 is etched to form a connection hole, and a polysilicon film is deposited on the insulating film 13 including the inside of the connection hole by the CVD method, followed by patterning the polysilicon film to be left on the upper portion of the connection hole thereby forming a lead-electrode 14.

Thereafter, a high melting metal film (not shown) such as titanium or the like is formed over the entire surface of the semiconductor substrate 1. Such a film may be made, aside from titanium, of a metal such as tungsten, cobalt or the like.

As shown in Fig. 3b, the semiconductor substrate 1 is subjected to thermal treatment by an RTA (rapid thermal annealing) method to form a silicide layer 16 at portions between the high melting metal film and the gate electrode 7 and also

between the lead electrode 14 and the semiconductor substrate 1. Subsequently, an unreacted high melting metal film is removed. Since these silicide layers 16 are formed, the connection resistance between the silicide layer 16 and a plug 21 or the like formed on the upper portion of the silicide layer 16 and described hereinafter can be reduced. In addition, the sheet resistance of the gate electrode 7 and the n<sup>+</sup>-type semiconductor region 11 or p<sup>+</sup>-type semiconductor region 12 per se can be reduced.

As shown in Fig. 4a, a silicon oxide film is deposited by the CVD method to form an interlayer insulating film 18. The interlayer insulating film 18 may be made of a PSG (phosphor silicate glass) or an SOG (spin on glass) film. The interlayer insulating film 18 may be flattened on the surface thereof by CMP. In this embodiment, the interlayer insulating film 18 is flattened by CMP on the surface thereof.

As shown in Fig. 4b, the interlayer insulating film 18 is removed by etching from the n<sup>+</sup>-type semiconductor region 11 or p<sup>+</sup>-type semiconductor region 12 and also from the silicide layer 16 constituting the resistor element R, thereby forming a contact hole 20.

Next, as shown in Fig. 5a, a titanium nitride film (not shown) is formed, by the CVD method, on the interlayer insulating film 18 including the contact hole 20, followed by further formation of a tungsten (W) film (i.e. a first conductive film defined in Claim 3). Next, the titanium nitride film (TiN) and

the tungsten film are removed by CMP from portions other than the contact hole 20. It will be noted that the titanium nitride film may be formed by a sputtering method. The titanium nitride film may be formed of laminated film of titanium (Ti) and titanium nitride (TiN).

As shown in Fig. 5b, a silicon nitride film 22 is formed over the interlayer insulating film 18 and the plug 21, followed by further deposition of a silicon oxide film 23 by the CVD method.

As shown in Fig. 6a, the silicon oxide film 23 is removed by etching from a region where a first wiring is to be formed, and the silicon nitride film 22 exposed by the etching is further etched to form a groove 25 for wiring. Accordingly, the etching of the silicon oxide 23 is performed under conditions where the silicon nitride film 22 is unlikely to be etched and the silicon oxide film 23 is likely to be etched. Thereafter, etching is carried out under conditions where the silicon nitride film 22 is likely to be etched. In this way, the silicon nitride film 22 is used as an etching stopper. In case where the degree of etching can be controlled such as by time, the silicon oxide film 23 may be formed directly on the silicon oxide film 18 without formation of the silicon nitride film 22.

Subsequently, as shown in Fig. 6b, a barrier layer 26a made of titanium nitride is deposited on the silicon oxide film 23 including the groove 25 for wiring by a sputtering method or a CVD method. A copper film 26b (i.e. a conductive film defined

in Claims 1, 18 and 19, a first conductive film defined in Claim 2, and a second conductive film defined in Claim 3) is formed (or attached) on the barrier layer 26a by a sputtering method. More particularly, a 0.4  $\mu\text{m}$  thick copper film 26b is formed at a flat portion under conditions including a distance between a target and a wafer of 300 mm, a film-forming pressure of 0.2 mTorr ( $0.2 \times 1.33322 \times 10^{-1}$  Pa) or below, a film-forming initial temperature of 20°C, and a final arrival temperature of 300°C, followed by annealing in a reductive atmosphere, or by treating in an atmosphere of hydrogen under conditions, for example, of 15 Torr ( $15 \times 1.33322 \times 10^2$  Pa) and 430°C for 2 minutes. The annealing in hydrogen is effected so as to reduce the oxide layer on the surface of the copper film and fluidize the copper film, thereby improving a burying characteristic of the copper in the wiring groove. The hydrogen (annealing) treatment leads to the improved quality of the copper film, and thus, the Cu wiring can be improved in reliability. It will be noted that the copper film may be formed (or attached) by an electroplating method. In this case, after formation of a thin copper film by a sputtering method, a metallic deposit may be grown while using such a thin film as a seed film. When the copper film deposited by plating is treated (annealed) with hydrogen, the copper film 26b can be improved in the quality thereof, thereby improving the reliability of the Cu wiring 26. The barrier layer 26a may be made not only of titanium nitride, but also a single-layered film

such as of tantalum (Ta), tantalum nitride (TaN), tungsten (W) or tungsten nitride (WN). Alternatively, there may be used, aside from a three-layered laminated film obtained by forming a titanium nitride film formed on a titanium film and further forming a titanium film (Ti/TiN/Ti), laminated films of Ti/TiN, Ta/TaN/Ta,, Ta/TaN and the like.

Next, as shown in Fig. 7a, the copper film 26b and the titanium nitride film 26a are, respectively, removed from the outside of the groove 25 for wiring by CMP to form a wiring 26.

Thereafter, tungsten is selectively or preferentially grown on the wiring 26 to form an approximately 2 to 20 nm thick tungsten film 26c (i.e. a cap conductive film defined in claims) on the wiring 26 (i.e. the copper film 26b). The tungsten film 26c is formed under conditions, for example, of 0.3 Torr ( $0.3 \times 1.33322 \times 10^2$  Pa), a preset temperature of 460°C, a flow rate of tungsten hexafluoride ( $WF_6$ ) of 5 scc., and a flow rate of hydrogen ( $H_2$ ) of 500 scc., for 1.5 minutes.

By the treatment, tungsten is selectively grown only on the wiring 26, or tungsten is preferentially grown on the wiring 26 in comparison with the silicon oxide film 18.

It will be noted that the selective growth or preferential growth can be achieved by the CVD method or plating method. When the film is formed by the CVD method, the conditions therefor include those of a film-forming pressure of 2 Torr ( $2 \times 1.33322 \times 10^2$  Pa) or below, a temperature of 250°C, and a ratio in flow

rate between tungsten hexafluoride ( $WF_6$ ) and hydrogen,  $WF_6/H_2$ , of 1/50 or below.

Aside from tungsten, there may be used, as the cap conductive film on the wiring 26, a TiN, Ta, TaN, WN or Ni film. The resistance of tungsten ranges from 5 to 20  $\mu Q \cdot cm$ , which is smaller than a resistance of TiN of 80 to 150  $\mu Q \cdot cm$ , so that the use of tungsten film ensures good contact at a low resistance.

Thus, according to this embodiment, since tungsten is formed on the wiring 26 by selective growth or preferential growth, the wiring 26 does not directly contact on the upper surface thereof with the insulating films such as the silicon nitride film and the silicon oxide film, but is in contact with the tungsten film 26c that is made of the same metal as the wiring, thereby permitting electromigration to be reduced. As stated hereinbefore, this is assumed for the reason that when comparing the interface between the copper and the barrier film with the interface between the copper and the silicon nitride film, the activation energy of diffusion is greater for the interface between the copper and the barrier film (i.e. copper is more unlikely to be diffused). Eventually, the wiring life can be improved.

The wiring 26 is covered at the side faces and bottom face thereof with the barrier layer 26a and at the upper face thereof with the tungsten film 26c. Thus, the wiring is covered wholly with the hard metals, and thus, the breakage of the wiring or

the like ascribed to stress migration can be prevented. As a result, the wiring life can be improved.

Even if a burying failure occurs in case where the copper film 26b is buried in the wiring groove 25, or if breakage, shrinkage or scratches are caused in the surface of the wiring 26 by CMP or a subsequent thermal treatment at the time of the formation of the wiring 26 (Fig. 22a), the formation of the tungsten film 26c on the surface of the wiring covers the defective portions such as a breakage, thereby permitting the defects to be repaired (Fig. 22b). It will be noted that Fig. 22a is a schematic view showing the case where a defect appears in the wiring 26, and Fig. 22b is a schematic view showing the state after the tungsten film has been selectively or preferentially grown on the wiring shown in Fig. 22a.

As stated hereinabove, the growth of an approximately 2 to 20 nm thick tungsten film is possible at a relatively low pressure (1 Torr ( $1 \times 1.33322 \times 10^2$  Pa) or below), and thus, the coverage on the surface of the wiring 26 is good, enabling small defects to be repaired.

These defects cause voids to occur, and electromigration is induced from such a void as a starting point, so that the repairing of the defect results in the reduction of electromigration. Eventually, the wiring life can be improved.

Next, as shown in Fig. 8a, a silicon nitride film 28 is formed on the silicon oxide film 23 and the wiring 26 (tungsten

film 26c), followed by further deposition of a silicon oxide film 29 by a CVD method.

Thereafter, the silicon oxide film 29 on the contact region of the wiring 26 is removed by etching, and the silicon nitride film 28 exposed by the etching is further etched to form a contact hole 30. Accordingly, the etching of the silicon oxide film should be effected under conditions where the silicon nitride film is unlikely to be etched and the silicon oxide film is apt to be etched. Thereafter, the silicon oxide 28 is etched under conditions where it is likely to be etched. In this way, the silicon nitride film 28 is utilized as an etching stopper, and where the degree of etching can be controlled such as by time, the silicon oxide film 29 may be formed directly on the silicon oxide film 23 and the wiring 26 without formation of the silicon nitride film 28. It will be noted that where any silicon nitride film cannot be used, the capacitance between the wirings can be reduced, resulting in the high-speed circuit operation.

For the formation of the contact hole 30 or for the etching of the contact hole at the bottom thereof as described hereinafter, the lower wiring 26 is covered with the tungsten film 26c whose surface is hard, so that copper is prevented from scattering at the time of sputtering etching. More particularly, where any tungsten film 26c is not formed, the wiring surface is etched as is particularly shown in Fig. 23a, and the scattered copper (SCu) is attached at the side of the contact hole 30. In contrast,



with the embodiment of the invention where the lower wiring 26 is covered with the tungsten film 26c whose surface is hard, copper is prevented from scattering as shown in Fig. 23b. Accordingly, a contaminated layer of copper is not formed at the lower portion of the barrier layer as described hereinafter, and thus, contamination of the silicon oxide film (insulating film) with copper can be prevented.

The use of the selective growth or preferential growth permits the tungsten film 26c to be readily formed on the surface of the wiring 26 (copper film 26c). When using the selective growth or preferential growth, the tungsten film 26c can be relatively uniformly irrespective of the wiring width. Moreover,, the film thickness can be made relatively uniformly (with a variation of 50% or below) throughout the wiring including the end and central portions thereof. When using the selective or preferential growth, the tungsten film 26c at the surface of the wiring 26 can be formed more thinly than the barrier layer 26a (especially, at the bottom thereof) covering the side walls and bottom of the wiring, ensuring a good contact characteristic with the upper wiring.

The silicon nitride film 28 on the surface of the wiring 26, which has been hitherto studied, is at least partially replaced by the tungsten film, so that the silicon nitride film 28 for preventing the diffusion of copper, which has a high dielectric constant and impedes a high-speed operation, can be

reduced in amount or disused, thus resulting in the high-speed operation of the device. More particularly, when comparing with the case using no tungsten film 26c, the silicon nitride film 28 can be reduced in its thickness, ensuring the high-speed operation of the device.

In the case where a void occurs beneath the plug 30 as described hereinafter and covers the contact region therewith, the tungsten film 26c serves as a current path, thereby establishing electric contact as shown in Fig. 24b. It will be noted that the hitherto studied silicon nitride film is formed on the surface of the wiring 26, the contact is impeded by means of a generated void as is particularly shown in Fig. 24a.

Fig. 29 is a view showing a resistance of a wiring after CMP of a copper film: A, after formation of a tungsten film: B and after formation of a silicon oxide: C. In this case, a silicon oxide is formed directly on the wiring, and any silicon nitride film is not used. The wiring resistance was measured prior to and after the formation of a tungsten film for two wiring widths (i.e. 0.4  $\mu\text{m}$  in width ( $\bigcirc$ ,  $\bullet$ ) and 0.8  $\mu\text{m}$  in width ( $\square$ ,  $\blacksquare$ ) in cases where the tungsten film was formed ( $\bullet$ ,  $\blacksquare$ ) and was not formed ( $\bigcirc$ ,  $\square$ ). The term "wiring resistance" used herein means a resistance of a wiring patterned with a length of 0.4  $\mu\text{m}$  and a length of 1 mm. As shown in Fig. 29, when the silicon oxide was formed after the formation of the tungsten film in case where the tungsten film was formed ( ,  $\blacksquare$ ), the resistance of the wiring

underwent little variation ( :  $140\Omega$  . ■:  $65\Omega$ ). In contrast, where the silicon oxide film was formed directly on the wiring without formation of a tungsten film, the wiring resistance extremely increased (○: from 140 to  $400\Omega$  . □: from 65 to  $180\Omega$ ).

This is considered for the reason that the wiring (i.e. copper film 26c) was oxidized at the contact between the wiring and the silicon oxide). In this way, the formation of the tungsten film 26c can prevent the surface of the wiring 26 from being oxidized, thereby reducing the rise of the wiring resistance.

Next, as shown in Fig. 8c, a plug 31 is formed inside the contact hole 30. In order to obtain a good contact characteristic prior to the formation of the plug 31, the contact hole is etched at the bottom thereof.

It will be noted that this etching or etching for making the contact hole 30 permits the tungsten film 26c at the bottom of the contact hole 30 to be also etched. The tungsten film 26c at the bottom of the contact hole may be lost by these etchings. Alternatively, the tungsten film 26c at the bottom of the contact hole may be separately etched.

The plug 31 is formed in the following manner. Initially, after formation of a titanium nitride film 31 by a CVD method or sputtering method on the silicon oxide 29 including the inside of the contact hole 30, a tungsten film 31b is formed according to a CVD method. Next, the titanium nitride film 31a and the



for the copper film 26b.

Next, the copper film 35b and the barrier layer 35a outside the wiring groove 34 are, respectively, removed by CMP to form a wiring 35.

Tungsten is subjected to selective growth or preferential grown on the wiring 35 (i.e. the copper film 35b) to selectively or preferentially form a tungsten film 35c on the wiring 35. The film-forming conditions are similar to those for the tungsten film 26c formed on the wiring 26.

As shown in Fig. 10, a silicon nitride film 36 is formed on the silicon oxide film 33 and the wiring 35 (i.e. the tungsten film 35c), followed by deposition of a silicon oxide film 27 by a CVD method.

Like the contact hole 30, the silicon oxide film 37 on the contact region of the wiring 35 is removed by etching, and the silicon nitride film 36 exposed by the etching is etched to form a contact hole 38.

Thereafter, like plug 31, a titanium nitride film 39a is formed on the silicon oxide film 37 including the inside of the contact hole 38 by a sputtering or CVD method, followed by formation of a tungsten film 39b by a CVD method. Next, the titanium nitride film 39a and the tungsten film 39b in areas other than the contact hole 38 are removed by CMP to form a plug 39. It will be noted that plug 39 may be made of a copper plug.

Further, a titanium film or titanium nitride film 40a,

an aluminium film 40b and a titanium nitride film 40c are successively deposited on the silicon oxide film 37 and the plug 39, followed by patterning the resultant laminated film in a desired form to form a wiring 40 extending over the plug 39.

As shown in Fig. 11, a silicon oxide film 41 is deposited on the wiring 40 and the silicon oxide film 37 by a CVD method, and an SOG film 42 is formed on the silicon oxide film 41. The formation of the SOG film 42 allows the irregularities caused by the wiring 40 to be flattened. It will be noted that a silicon oxide film 42a such as a TEOS film or the like may be formed on the SOG film 42 by a CVD method.

The silicon oxide film 42a, SOG film 42 and silicon oxide film 41 are removed by etching from the contact area of the wiring 40. Subsequently, an aluminium film is deposited on the contact area of the wiring 40 and the silicon oxide film 42a by a sputtering method, followed by patterning in a desired form to form a wiring 43.

Thereafter, a silicon nitride film 44 is formed on the wiring 43, and a silicon oxide film 45 is formed on the silicon nitride film 44. These silicon nitride film 44 and silicon oxide film 45 function as a passivation film for preventing penetration of moisture and impurities from outside or suppressing transmission of an  $\alpha$  ray.

The silicon oxide film 45 and the silicon nitride film 44 are, respectively, removed by etching to permit part of the

wiring 43 (i.e. a bonding pad portion) to be exposed.

Subsequently, a bump underlying electrode 47, which is made of a laminated film such as of a gold film, a nickel film and the like, is formed on the exposed wiring 43, followed by formation of a bump electrode 48, made of gold, a solder or the like, on the bump underlying electrode 47.

Thereafter, the resultant device is packaged in a package substrate to complete a semiconductor integrated circuit device, and the illustration for this is omitted herein.

In the embodiment described hereinabove, the wiring 26 is formed as a first layer wiring and the wiring 35 is formed as the second layer wiring, and the aluminium wiring 40 is formed on the second layer wiring via the plug 39. Alternatively, as shown in Fig. 12, a third layer wiring M3 and a fourth layer wiring M4 may be formed between the second layer wiring 35 and the aluminium wiring 40. In such a case, the third layer wiring M3 and the fourth layer wiring M4 may be, respectively, formed like the first and second layer wirings 26, 35 wherein tungsten films M3c, M4c are, respectively, formed on the wiring surface. A plug P3 between the third layer wiring and the fourth layer wiring and a plug P4 between the fourth layer wiring and the aluminium wiring 4 may be, respectively, formed in the same manner as the plugs 31, 39. Reference numerals 49, 51, 53 and 55, respectively, indicate a silicon nitride film, and reference numerals 50, 52, 54 and 56, respectively, indicate a silicon oxide film.

In this embodiment, the tungsten films 26c, 35c are selectively or preferentially grown on the wirings 26, 35, respectively, and the tungsten films may be selectively or preferentially grown in the plugs 31, 39, respectively.

#### Embodiment 2

In Embodiment 1, the wirings are formed according to a so-called single damacene method wherein the wiring is formed at the step different from the step of forming a plug connecting the wirings therewith, and may be formed according to a dual damacene method. Figs. 13 to 20 are, respectively, sectional views showing, one by one, the steps of a method of manufacturing a semiconductor integrated circuit device according to Embodiment 2 of the invention. The steps up to the formation of the plug 21 illustrated with reference to Figs. 1a to Fig. 6a are similar to those of Embodiment 1 and are not repeatedly described herein.

The semiconductor substrate 1 shown in Fig. 6a is formed thereon with the n-channel MISFET  $Q_n$  and the p-channel MISFET  $Q_p$ , which are, respectively, provided with the source and drain having the LDD (lightly doped drain) structure on the p-type well 3 and the n-type well 4, and also with a resistor element including, on the wide element isolation region 2, the conductor R, the insulating film 13 covering the conductor film R therewith and the lead electrode 14 on the insulating film 13. Moreover, the interlayer insulating film 18 is formed over the semiconductor



elements, and the plug 21 that reaches the source-drain regions of the MISFET's and the resistor element is formed in the interlayer insulating film 18.

Such a semiconductor substrate 1 as mentioned above is provided, and, as shown in Fig. 13a, a silicon nitride film 22 is formed over the interlayer insulating film 18 and the plug 21, followed by deposition of a silicon oxide film 23 by a CVD method.

Next, as shown in Fig. 13b, the silicon oxide film is removed by etching from a region where a first layer wiring is to be formed, and the silicon nitride layer 22 exposed by the etching is further etched to form a groove 25 for wiring. Accordingly, the etching of the silicon oxide layer 23 is performed under conditions where the silicon nitride film 22 is unlikely to be etched and the silicon oxide film 23 is likely to be etched. Thereafter, etching is carried out under conditions where the silicon nitride film 22 is likely to be etched. In this way, the silicon nitride film 22 is used as an etching stopper. In case where the degree of etching can be controlled such as by time, the silicon oxide film 23 may be formed directly on the silicon oxide film 18 without formation of the silicon nitride film 22.

Subsequently, as shown in Fig. 14a, a barrier layer 26a made of titanium nitride is deposited on the silicon oxide film 22 including the groove 25 for wiring by a sputtering or CVD method.

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A copper film 26b is formed on the barrier layer 26a by a sputtering method. More particularly, a 0.4  $\mu\text{m}$  thick copper film 26b is formed at a flat portion under conditions including a distance between a target and a wafer of 300 mm, a film-forming pressure of 0.2 mTorr ( $0.2 \times 1.33322 \times 10^{-1}$  Pa) or below, a film-forming initial temperature of 20°C, and a final arrival temperature of 300°C, followed by annealing in a reductive atmosphere, or by treating in an atmosphere of hydrogen under conditions, for example, of 15 Torr ( $15 \times 1.33322 \times 10^2$  Pa) and 430°C for two minutes. This hydrogen treatment is effected so as to reduce the oxide layer on the surface of the copper film and fluidize the copper film, thereby improving a burying characteristic of the copper in the wiring groove. The treatment with hydrogen leads to the improved quality of the copper film, and thus, the Cu wiring 26 can be improved in reliability.

It will be noted that the copper film 26b may be formed by an electroplating method. In this case, after formation of a thin copper film by a sputtering method, a metallic deposit may be grown while using such a thin film as a seed film. More particularly, a 200 nm thick copper film is formed at a flat portion under conditions including a distance between a target and a wafer of 300 mm, a film-forming pressure of 0.2 mTorr ( $0.2 \times 1.33322 \times 10^{-1}$  Pa) or below, a film-forming initial temperature of 10°C, and a final arrival temperature of 50°C. Thereafter, the semiconductor substrate 1 is immersed in a plating solution

based on sulfuric acid and copper sulfate. The semiconductor substrate 1 is applied with a negative potential for electroplating until a 600 nm thick copper film is formed at a flat portion. Fig. 14a shows the state of the copper film 26b formed by this electroplating method. The seed film may be formed by a CVD method. This copper film 26b is treated with hydrogen in the same manner as set out above. The hydrogen treatment leads to an improved quality of the copper film 26b, thereby improving the reliability of the Cu wiring.

The barrier layer 26a may be made not only of titanium nitride, but also a single-layered film such as of tantalum, tantalum nitride, tungsten or tungsten nitride. Alternatively, there may be used, aside from a three-layered laminated film obtained by forming a titanium nitride film formed on a titanium film and further forming a titanium film (Ti/TiN/Ti), laminated films of Ti/TiN, Ta/TaN/Ta,, Ta/TaN and the like.

Next, as shown in Fig. 14b, the copper film 26b and the barrier layer 26a are, respectively, removed from the outside of the groove 25 for wiring by CMP to form a wiring 26.

Thereafter, tungsten is selectively or preferentially grown on the wiring 26 (i.e. the copper film 26b) to form an approximately 2 to 20 nm thick tungsten film 26c on the wiring 26 (i.e. the copper film 26b). The tungsten film 26c is formed under conditions, for example, of 0.3 Torr ( $0.3 \times 1.33322 \times 10^2$  Pa), a preset temperature of 460°C, a flow rate of tungsten

hexafluoride ( $WF_6$ ) of 5 scc., and a flow rate of hydrogen ( $H_2$ ) of 500 scc., for 1.5 minutes.

By the treatment, tungsten is selectively grown only on the wiring 26, or tungsten is preferentially grown on the wiring 26 in comparison with the silicon oxide film 18.

It will be noted that aside from tungsten, there may be used, as the cap conductive film on the wiring 26, a TiN, Ta, TaN, WN or Ni film. The resistance of tungsten ranges from 5 to 20  $\mu Q \cdot cm$ , which is smaller than a resistance of TiN of 80 to 150  $\mu Q \cdot cm$ , so that the use of tungsten film ensures good contact at a low resistance.

Thus, according to this embodiment, since tungsten is formed on the wiring 26 by selective growth or preferential growth, the wiring 26 does not directly contact on the upper surface thereof with the insulating films such as the silicon nitride film and the silicon oxide film, but is in contact with the tungsten film 26c that is made of the same metal as the wiring, thereby permitting electromigration to be reduced. As stated hereinbefore, this is assumed for the reason that when comparing the interface between the copper and the barrier film with the interface between the copper and the silicon nitride film, the activation energy of diffusion is greater for the interface between the copper and the barrier film (i.e. copper is more unlikely to be diffused). Eventually, the wiring life can be improved.

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The wiring 26 is covered at the side faces and bottom face thereof with the barrier layer 26a and at the upper face thereof with the tungsten film 26c. Thus, the wiring is covered wholly with the hard metals, and thus, the breakage of the wiring or the like ascribed to stress migration can be prevented. As a result, the wiring life can be improved.

Even if a burying failure occurs in case where the copper film 26b is buried in the wiring groove 25, or if breakage, shrinkage or scratches are caused in the surface of the wiring 26 by CMP or a subsequent thermal treatment at the time of the formation of the wiring 26 (Fig. 22a), the formation of the tungsten film 26c on the surface of the wiring covers the defective portions such as a breakage, thereby permitting the defects to be repaired (Fig. 22b).

As stated hereinabove, the growth of an approximately 2 to 20 nm thick tungsten film is possible at a relatively low pressure (1 Torr ( $1 \times 1.33322 \times 10^2$  Pa) or below), and thus, the coverage on the surface of the wiring 26 is good, enabling small defects to be repaired.

These defects cause voids to occur, and electromigration is induced from such a void as a starting point, so that the repairing of the defect results in the reduction of electromigration. Eventually, the wiring life can be improved.

Next, as shown in Fig. 15b, a silicon nitride film 28, a silicon oxide film 29, a silicon nitride film 32 and a silicon

oxide film are successively formed on the silicon oxide film 23 and the wiring 26 by a CVD method. The silicon nitride film 32 serves as an etching stopper when the wiring groove 34 is formed, and the silicon nitride film 28 functions as an etching stopper when a contact hole 30 for connection with the lower wiring 26 is formed.

Next, as shown in Fig. 16a, the silicon oxide film 33, silicon nitride film 32 and silicon oxide film 29 are, respectively, removed by etching from the contact region of the wiring 26, and the silicon nitride film 28 exposed by the etching is etched to form a contact hole 30.

Thereafter, as shown in Fig. 16b, an anti-reflecting film or resist film 33a is formed on the silicon oxide film 33 including the inside of the contact hole 30 to bury the contact hole with the anti-reflecting film or resist film 33a. Further, as shown in Fig. 17a, the anti-reflecting film or resist film 33a and the silicon oxide film 33 are etched through the mask of a photoresist film (not shown) having an opening for a region where a second layer wiring is to be formed. Subsequently, the silicon nitride film 32 exposed by the etching is etched to form a groove 34 for wiring. At that time, the anti-reflecting film or resist film 33a remains in the contact hole. Thereafter, the anti-reflecting film or resist film 33a left in the contact hole and the photoresist film are removed.

According to the steps set forth above, the wiring groove

34 for second layer wiring and the contact hole 30 connecting a second layer wiring and the first layer wiring therewith are formed as shown in Fig. 17b.

The contact hole 30 may be formed by etching the silicon oxide film 33 and the silicon nitride film 32 through the mask of the photoresist film having an opening for a region where a second layer wiring is to be formed, thereby forming a groove 34 for wiring, burying the wiring groove 34 with an anti-reflecting film or the like, and etching the anti-reflecting film, silicon oxide film 29 and silicon nitride film 28 through a mask of a photoresist film having an opening for the contact region on the first layer wiring.

The silicon nitride films 32, 28 used as an etching stopper may not be used when the degree of etching can be controlled such as by time. More particularly, a silicon oxide film having a total thickness of the silicon oxide films 29 and 33 formed on the silicon oxide 23 and the wiring 26 is formed. The silicon oxide is etched for a given time through a mask of a resist film having an opening for a region where a second layer wiring is to be formed thereby forming a groove 34 for wiring, followed by formation of the contact hole 30 through a mask of a resist film having an opening for the contact area on the first layer wiring. In this case, after the formation of the contact hole 30, the wiring groove 34 may be formed.

After the formation of the silicon oxide film 29 (called







5 scc., and a flow rate of  $H_2$  of 500 scc., for 1.5 minutes.

According to such a treatment as mentioned above, tungsten is selectively or preferentially grown only on the wiring 35 (copper film 35b), or tungsten is preferentially grown on the wiring 35 rather than the silicon oxide film 34.

Copper is prevented from scattering when the contact hole 30 is formed or the contact hole 30 is etched at the bottom thereof, or at the time of sputtering etching. This is like the case of Embodiment 1 as described with reference to Fig. 23.

The use of the selective growth or preferential growth allows easy formation of the tungsten film on the surface of the wiring 35. Thus, a relatively uniform tungsten film can be formed on the surface of the wiring as illustrated in Embodiment 1. When using the selective growth or preferential growth, the tungsten film on the wiring surface can be formed thinly, leading to the advantages that a good contact characteristic is obtained, that the silicon nitride film on the surface of the copper film, which has a high dielectric constant and impedes the high-speed operation, can be substituted with the tungsten film, thus realizing the high-speed operation of the device, and that in case where a void occurs in the vicinity of a plug described hereinafter covers the contact region therewith, the tungsten film serves as a current path, ensuring the contact (see Fig. 24). These advantages are just as described in Embodiment 1.

Further, as described in Embodiment 1 while referring to

Fig. 29, the formation of the tungsten film 35c can prevent the surface of wiring 35 from being oxidizing, reducing the rise of the wiring resistance.

It may occur that there is formed on the copper wiring TiN, Ta, TaN, WN or Ni, aside from tungsten. The resistance of tungsten is at 5 to 20  $\mu\Omega\cdot\text{cm}$  that is small than TiN whose resistance is at 80 to 150  $\mu\Omega\cdot\text{cm}$ , so that the use of a tungsten film contributes to the good contact.

Next, as shown in Fig. 20, a silicon nitride film 36 and a silicon oxide film 37 are successively formed on the silicon oxide film 33 and the wiring 35 by a CVD method, respectively. Thereafter, a plug 39 is formed to further form a wiring 40. These formation steps are similar to those of Embodiment 1 and are not described in more detail. Moreover, a wiring 43 formed on the wiring 40 via a silicon oxide film 41, and a bump underlying electrode 47 and a bump electrode 48 formed on the wiring 43 via a silicon nitride film 44 and a silicon oxide film 45 are, respectively, formed in the same manner as in Embodiment 1, for which detailed description therefor is not made herein.

After the formation of the bump electrode 48, the resultant device is packaged in a package substrate or the like to complete a semiconductor integrated circuit device, which is not described herein.

In this embodiment, although the first layer wiring 26 and the second layer wiring 35 are formed, and the aluminium

wiring 40 is formed on the second layer wiring 35 through the plug 39, a third layer wiring M3 and a fourth layer wiring M4 may be formed between the second layer wiring and the aluminium wiring 40 (Fig. 21), like Embodiment 1. In such a case, the third layer wiring and the fourth layer wiring are formed according to the dual damacene method, like the first and second layer wirings. More particularly, after the formation of a wiring groove and a contact hole, these are simultaneously buried to form the wirings. The wirings are formed on the surfaces thereof with tungsten films (3Mc, 4Mc).

#### Embodiment 3

In Embodiments 1 and 2, after the formation of the tungsten films 26c, 35c (see Fig. 7b in Embodiment 1 and Fig. 19 in Embodiment 2), the silicon nitride films 28, 36 and the silicon oxide films 29, 37 are formed on the tungsten films 26c, 35c, respectively. Alternatively, as shown in Figs. 25a and 25b, silicon oxide films (hereinafter referred to as TEOS film) 328, 336, which are deposited according to a CVD method using tetraethoxysilane as a starting gas, are thinly formed on the tungsten films 26c, 35c, respectively, followed by further formation thereon of insulating films 329, 337 having a dielectric constant lower than the TEOS films (i.e. a dielectric constant of 4 or below). It will be noted that a carbon-containing silicon-based insulating film, such as a silicon carbide film, an SiCO film or the like, may be used in place of the TEOS films

328, 336. The carbon-containing silicon-based insulating film such as SiC or SiCO has a dielectric constant as low as  $\epsilon \approx 4$  to 6, and serves as a diffusion-preventing (barrier) layer for Cu, like a silicon nitride (SiN) film.

If the TEOS films 328, 336 are formed on the tungsten films 26c, 35c, respectively, the wirings 26, 35 can be protected by means of the dense TEOS films. When the insulating films 329, 337 whose dielectric constant is low are formed, the high-speed operation of the semiconductor integrated circuit is ensured. When the carbon-containing silicon-based insulating films 328, 336, such as a SiC film or a SiCO film, are, respectively, formed on the tungsten films 26c, 35c, these films are lower in dielectric constant ( $\epsilon \approx 4$  to 6) than a silicon nitride film and serves as a Cu diffusion barrier, like the silicon nitride film, thus resulting in the high-speed operation and high reliability of the resultant semiconductor integrated circuit device.

It will be noted that the steps up to the formation of the tungsten films 26c, 35c are similar to those illustrated with respect to Embodiment 1 or 2, and their illustration is not repeated herein.

The steps subsequent to the formation of the insulating films 329, 337 are similar to those steps after the formation of the silicon oxide films 29, 37 in Embodiments 1 and 2, and are not repeated.

Embodiment 4

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In Embodiments 1 to 3, after the formation of the tungsten films 26c, 35c (see Fig. 7b in Embodiment 1 and Fig. 19 in Embodiment 2), the silicon nitride films 28, 36 and the silicon oxide films 29, 37 are, respectively, formed on the tungsten films 26c, 35c. Instead, as shown in Figs. 26a and 26b, insulating films 428, 436, which include a silicon nitride film, a PSG film, or a carbon-containing silicon-based insulating film such as a silicon carbide (SiC) film or a SiCO film and which have the capability of preventing diffusion of copper, may be formed on the tungsten films 26c, 35c. Moreover, insulating films 429, 437 made of a low dielectric material having a dielectric constant lower than the insulating films 428, 436 are formed on the tungsten films 26c, 35c, respectively. The insulating films 429, 437 made of the low dielectric material include, for example, those insulating films having a dielectric constant of 4 or below, such as a TEOS film, a SiOF film, an organic coating film, and a porous silica film.

The formation of the silicon nitride films 428, 436 on the tungsten films 26c, 35c can prevent copper from diffusion into the silicon nitride films 428, 436 and the TEOS films 429, 436 by means of the silicon nitride films 428, 436 even at a portion where the thickness of the tungsten films 26c, 35c is not sufficient for the prevention. Because the TEOS films 429, 437 have a dielectric constant of 4 or below and are thus relatively low in the dielectric property, the dielectric constant of the

insulating films as a whole can be lowered. Thus, the high-speed operation of the resulting semiconductor integrated circuit device is ensured. When using silicon carbide films or SiCO films as 428, 436, which are a carbon-containing silicon-based insulating film, the dielectric constant of the insulating films as a whole can be lowered and such films serve as a barrier layer against diffusion of Cu. Thus, the high-speed operation of the semiconductor integrated circuit device is realized with improved reliability.

It will be noted that the steps up to the formation of the tungsten films 26c, 35c are similar to those steps illustrated with respect to Embodiment 1 or 2 and are not repeatedly illustrated.

The steps subsequent to the formation of the insulating films 429, 437 made of a low dielectric material are similar to the steps after the formation of the silicon oxide films 29, 37 in Embodiments 1 and 2 and are not repeatedly illustrated.

#### Embodiment 5

In Embodiments 1 to 4, after CMP of the copper films 26b, 35b, the tungsten films 26c, 35c are selectively or preferentially grown on the surface the wirings 26, 35. Prior to the formation of the tungsten films 26c, 35c, the following pretreatment may be performed.

After CMP of the copper films 26b, 36b (see Fig. 7a in Embodiment 1 and Fig. 18b in Embodiment 2), the substrate surfaces





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a hydrogen fluoride (HF) solution is effected (A), the yield is at about 30%. In contrast, in cases where cleaning with a hydrogen fluoride (HF) solution is effected for a time of 20 seconds (B) and 60 seconds (C), the yield is at 100%. Thus, the yield including a wiring short-circuiting yield can be remarkably improved.

The pretreatment in this embodiment may be applied to the manufacture of the semiconductor integrated circuit devices illustrated in Embodiments 1 to 4. Moreover, the pretreatment in this embodiment can remove foreign matters or contaminant metals in case where the tungsten films 26c, 35c used as a barrier layer are not provided on the Cu wirings 26, 35, respectively, thus improving the yield such as a wiring short-circuiting yield. More particularly, as shown in Fig. 7a, after CMP of the copper films 26b, 35b, the substrate surfaces are cleaned with a solution for removing foreign matters or contaminant metals as in this embodiment, i.e. the solution containing at least one of HF, HCl, H<sub>2</sub>SO<sub>4</sub>, H<sub>2</sub>O<sub>2</sub>, citric acid, oxalic acid, ammonia and aminoethanol. Thereafter, as shown in Fig. 8a, the silicon nitride film 28 is formed. In this way, foreign matters and contaminant metals are removed, thereby improving a yield such as a wiring short-circuiting yield. If the tungsten films 26c, 35c are cleaned with such a cleaning solution as mentioned above prior to and after selective growth, a yield such as a wiring short-circuiting yield can be further improved.

## Embodiment 6

In Embodiments 1 and 2, after CMP of the copper films 26b, 35b and the like, the tungsten films 26c, 35c are selectively or preferentially grown on the surfaces of the wirings 26, 35. Prior to the formation of the tungsten films 26c, 35c, the following pretreatment may be carried out.

After completion of CMP of the copper films 26b, 35b (see Fig. 7a in Embodiment 1 and 18b in Embodiment 2), the substrate surfaces are treated with hydrogen or annealed under conditions, for example, of 430°C and 10 Torr ( $10 \times 1.33322 \times 10^2$  Pa). The hydrogen treatment may be effected within an apparatus for the formation of the tungsten films 26c, 35c.

Thus, when the substrate surfaces are subjected to hydrogen treatment prior to the selective or preferential growth of the tungsten films 26c, 35c on the wirings 26, 35, the oxide on the wirings is reduced, and an adsorbed gas, moisture and organic matter can be removed from the substrate surfaces. When hydrogen is adsorbed or occluded on or in the wiring surface, tungsten is more likely to be selectively or preferentially grown at the subsequent formation of the tungsten films 26c, 35c.

Accordingly, there can be formed highly reliable tungsten films, and adherence between the tungsten films and the copper films 26b, 35b can be improved.

Fig. 28b is a graph showing a wiring short-circuiting yield for the cases where the hydrogen treatment is effected for a

treating time of 60 seconds (B) and 300 seconds (C) and for the case where no hydrogen treatment is effected. Fig. 28c is a graph showing a wiring resistance yield. It will be noted that the growth conditions of the tungsten film include a preset temperature of 460°C, a flow rate of WF<sub>6</sub> of 7 scc., a flow rate of hydrogen of 500 scc., a pressure of 0.45 Torr (0.45 x 1.33322 x 10<sup>2</sup> Pa) and a treating time of 120 seconds. The cleaning treatment illustrated in Embodiment 5 and Embodiment 7 appearing hereinafter

As shown in Fig. 28b, the case where no hydrogen treatment is effected (A), the wiring short-circuiting yield is substantially at 0%. The cases where the hydrogen treatment is effected for a treating time of 60 seconds (B) and 300 seconds (C), respectively, have both a yield of 100%. Moreover, as shown in Fig. 28c, with the case where no hydrogen treatment is effected (A), the wiring resistance yield is at approximately 30%. Where the hydrogen treatment is effected for a treating time of 60 seconds (B) and 300 seconds (C), the yield is both at 100%. Thus, the yields such as the wiring resistance yield can be improved. Moreover, as shown in Fig 6b, the reliability of the Cu wiring 26 can be further improved when the hydrogen (annealing) treatment is effected after the formation of the copper film and also after CMP of the copper film. In addition, where any tungsten films 26c, 35c are not formed, the hydrogen (annealing) treatments after deposition of the copper film and after CMP of

the copper film ensure more improved reliability of the Cu wiring 26.

If a similar reduction treatment is effected, e.g. an ammonia ( $\text{NH}_3$ ) plasma treatment is effected at  $360^\circ\text{C}$ , after the formation of the tungsten films 26c, 35c, an adsorbed gas, moisture and organic matter can be removed from the substrate surfaces including the surface of the tungsten films 26c, 35c, thereby forming highly reliable tungsten films. Of course, the adherence with an insulating film, such as a silicon nitride film, formed on the tungsten films 26c, 35c can be improved. It will be noted that this reduction treatment may be carried out within the same apparatus as used for the formation of the insulating film.

The pretreatment in this embodiment can be applied to for the manufacture of the semiconductor integrated circuit devices illustrated in Embodiments 3 to 5.

If the cleaning treatment illustrated in Embodiment 5 and the reduction treatment of this embodiment are used in combination for the manufacture of the semiconductor integrated circuit devices illustrated with respect to Embodiments 1 to 4, the yields can be further improved, with more improved reliability of the wirings. More particularly, when the hydrogen (annealing) treatment after deposition of the copper film and the cleaning treatment, which has been illustrated with respect to Embodiment 5, after CMP of the copper film are

performed, after which when the hydrogen (annealing) treatment is effected, the reliability of the Cu wiring can be further improved.

#### Embodiment 7

After the selective or preferential growth of the tungsten films 26c, 35c on the wiring surface, the following after-treatment may be carried out.

After the selective or preferential growth of the tungsten films 26c, 35c on the surfaces of the wirings 26, 35 (see Fig. 7b in Embodiment 1 and Fig. 19a in Embodiment 2), the substrate surfaces (including the surfaces of the tungsten films 26c, 35c and the silicon oxide films 23, 33, and the like) are cleaned with a solution capable of removing contaminant metals and containing at least one of hydrogen fluoride (HF), hydrogen peroxide ( $H_2O_2$ ), citric acid and the like as mentioned hereinbefore.

When the substrate surfaces are cleaned with a hydrogen fluoride (HF) solution or the like after the selective or preferential growth of the tungsten films 26c, 35c, a tungsten film is grown on the silicon oxide film (i.e. breakage of the selectivity occurs) as shown in Fig. 27a. If a tungsten film is grown on a contaminant metal on the silicon oxide film as illustrated with regard to Embodiment 5, these unnecessary tungsten film and contaminant metal are etched, thereby providing a highly reliable tungsten film.

For the removal of the unnecessary tungsten film, CMP may be used. While the tungsten film formed on a wiring is a relatively thick and continuous film, a tungsten film formed on an insulating film is discontinuous and thin, so that only the tungsten film on the insulating film can be removed.

The after-treatment in this embodiment can be applied for the manufacture of the semiconductor integrated circuit devices illustrated in Embodiments 1 to 6.

When the pretreatment illustrated in Embodiment 5 or 6 and the after-treatment of this embodiment are used in combination for the manufacture of the semiconductor integrated circuit devices illustrated in Embodiments 1 to 4, the yield and reliability of the wiring can be further improved.

Moreover, the cleaning treatment illustrated in Embodiment 5, the reduction treatment illustrated in Embodiment 6 and the after-treatment of this embodiment are used in combination for the manufacture of the semiconductor circuit devices illustrated in Embodiments 1 to 4, the yield and reliability of the wiring can be further improved.

The invention made by us has been particularly described based on the embodiments, which should not be construed as limiting the invention. Many alterations and modifications may be possible within the scope of the invention.

Especially, in the foregoing embodiments, a copper wiring (copper film 26b) is used, and the wiring may be made of, aside

from copper, silver, aluminium or an alloy mainly comprised of these metals. The copper alloys include an alloy having a Mg content of 5% or below, or an alloy having an Al content of 3% or below.

In the foregoing embodiments, the copper films 26b, 35b are formed on the barrier layers 26a, 35a, respectively. As shown in Fig. 30, many alterations and combinations are possible including (a) tungsten films 826a, 835a left only at the bottom of the wiring groove, (b) tungsten film 835d formed further on the barrier film 35a, and (c) barrier layers 26a, 35a further formed on the tungsten films 826a, 835a indicated (a) above.

The effects, advantages and features attained by typical embodiments of the invention disclosed herein are briefly described below.

According to the method for manufacturing a semiconductor integrated circuit device of the invention, a cap conductive film is selectively or preferentially grown on a wiring, thus leading to a high-speed operation of the semiconductor integrated circuit device.

Occurrence of electromigration and stress migration can be suppressed and thus, a wiring life can be elongated.

Moreover, when the contact hole formed on the wiring is etched at the bottom thereof, the underlying wiring can be prevented from direct sputtering, so that a breakdown voltage can be improved, with a reduced leakage current.

If the contact hole is shifted relative to a wiring, contact can be maintained, with a reduction in number of contact failures.

The oxidation of a wiring surface can be suppressed, thereby reducing the rise of a wiring resistance.

If a pretreatment is effected, e.g. the substrate surfaces is cleaned with a solution containing HF (hydrogen fluoride) or the like, or the substrate surfaces are treated with hydrogen, prior to the formation of the cap conductive film, there can be formed a highly reliable cap conductive film. When the substrate surfaces are cleaned with a solution containing hydrogen fluoride (HF) or hydrogen peroxide ( $H_2O_2$ ) after formation of the cap conductive film, a highly reliable cap conductive film can be formed.

The semiconductor integrated circuit device of the invention is formed with a cap conductive film on a wiring, so that the high-speed operation thereof is realized.

Electromigration or stress migration is suppressed from occurring, and thus, an elongated wiring life is ensured.

Moreover, when the contact hole formed on the wiring is etched at the bottom thereof, the underlying wiring can be prevented from direct sputtering, so that a breakdown voltage can be improved, with a reduced leakage current.

If the contact hole is shifted relative to a wiring, contact can be maintained, with a reduction in number of contact



failures.

The oxidation of a wiring surface can be suppressed, thereby reducing the rise of a wiring resistance.

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